

**ABSTRACT**

A circuit for controlling a memory including at least two areas to which access cannot be had simultaneously, the circuit including first circuitry for storing a series of read and/or write instructions separately for each of the areas, and second circuitry for detecting that a  
5 first instruction intended for a first area is a predetermined instruction to be followed by a period during which the first area can receive no other instruction, and third circuitry for, during the period, providing instructions to another memory area.